RTAX-S Field Programmable Gate Array (FPGA) Risk Reduction Testing

Brian Smith

BSmith@SpaceFPGAs.com 301-358-2582

Task Description

RTAX-S Field Programmable Gate Array (FPGA) Risk Reduction Test Results Status Report, (NESC Task 06-010-E)

SCOPE: A small Agency-wide team with relevant expertise will be formed to evaluate the RTAX-S FPGA Test Plan and provide a technical assessment.

TEAM: Task lead by NESC (Brian Smith) with team members/consultants from LaRC, GRC, GSFC, MSFC, JSC, JPL, APL, NEPP, Aerospace Corp. & Sandia National Labs.

Original Proposal by Rich Katz, NASA GSFC

Test Objectives

Test RTAX Parts with representative user designs

- Motivation:
  - Many current and upcoming NASA programs are planning to fly Actel RTAX parts
  - Advances in density, functionality, and packaging (and hopefully reliability) over current programmable parts make them attractive to digital designers.

Test Objectives

- Motivation (cont'd.)

- Actel QBI (Qualification Burn In) tests target previously discovered and common CMOS issues.

- Aerospace tests are targeted to:
  - antifuse stress, memory functionality and reliability
  - structure reliability
  - using commercial equivalent parts (similar physics)

- Several Million Device Hours Completed

Test Objectives

- Motivation (cont'd.)
  - This test is intended to find failure mechanisms that have NOT been seen before.
  - Even after QBI and reliability testing, faults can be found through the unique designs users will implement in the parts.
  - This test is intended to simulate the user environment, with the goal of finding any hidden issues early in NASA's use of RTAX parts for flight programs.

Test Objectives

- Perform Life Testing on a large number of flight parts
- Use designs representative of those used in flight
- Trend parametric data for future use
- Log, analyze, and characterize and failures
- Develop guidance for flight projects if any anomalies or peculiarities are discovered during the development or life testing

Parts Tested

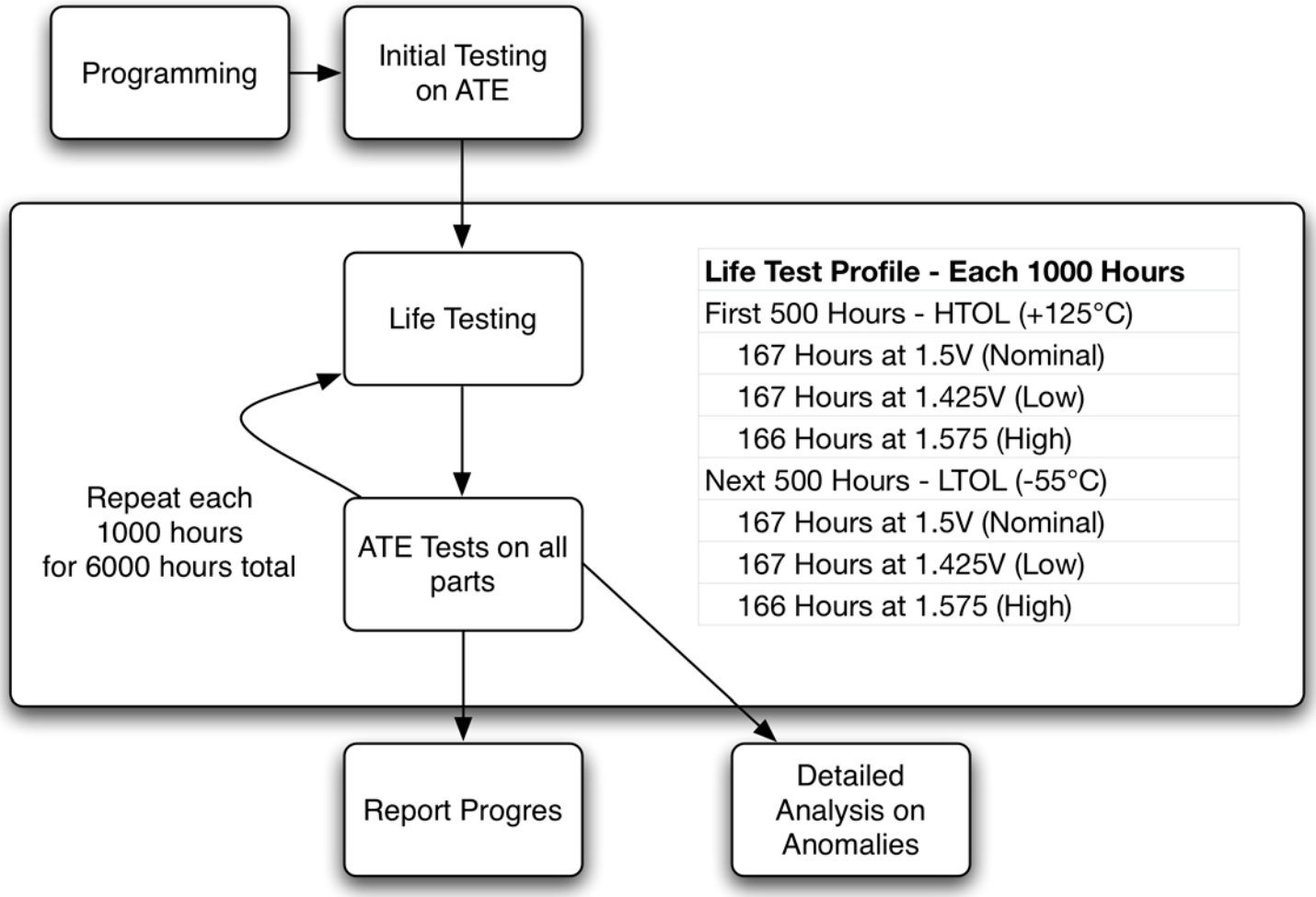
- **PART Specifics**:
  - RTAX250S-CQ208BX200
    - 80 Parts, 40 from each of two lots
  - RTAX2000S-LG624BX200
    - 80 Parts, 40 from each of two lots
- These are the most commonly selected FPGAs for new space designs

Test Plan

- **Design Specifics:**
  - 6000 Hour Test
  - Uses Actel-supplied test boards
  - Self-testing designs
  - Multiple designs in test chip

- **Logistics:**
  - Tests performed at Actel facility
  - Periodic test monitoring by NASA personnel
  - Interim status reports as tests progress

Test Flow


Programming
Initial Testing on ATE
Life Testing
ATE Tests on all parts
Repeat each 1000 hours for 6000 hours total
Report Progres
Detailed Analysis on Anomalies
Life Test Profile - Each 1000 Hours
First 500 Hours - HTOL (+125°C)
167 Hours at 1.5V (Nominal)
167 Hours at 1.425V (Low)
166 Hours at 1.575 (High)
Next 500 Hours - LTOL (-55°C)
167 Hours at 1.5V (Nominal)
167 Hours at 1.425V (Low)
166 Hours at 1.575 (High)

Designs

- Selected Representative Designs :
  - 1553 Remote Terminal (Sital Technology)
  - 8-bit processor (PIC 16F84)
  - EDAC
  - Memory Controller / Scrubber
  - UART
- Designs were chosen by planned use in NASA programs, completeness of source and test code, FPGA resources required.
- Error Block collects error signal from each block and signals error to test board.

Test Chip - RTAX2000S

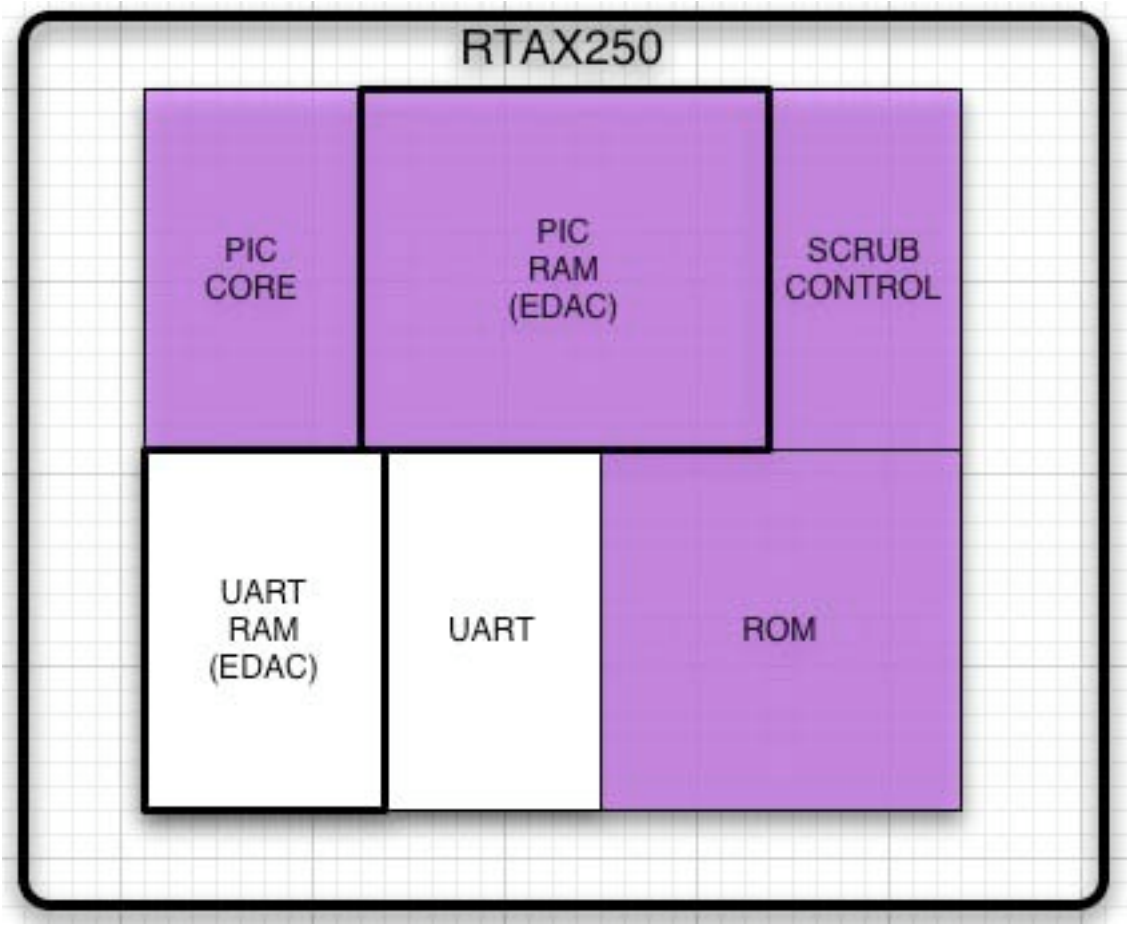
- 5 PIC Processors
- 3 UARTs
- 3 1553 Self-Test Cores
- ERROR/Control Block

Combinational Cells:
18171 of 21504 (85%)
Sequential Cells:
7545 of 10752 (70%)
Total Cells:
25716 of 32256 (80%)
Clock Buffers: 8
IO Cells: 39

Test Chip - RTAX250S

- 1 PIC Processor
- 1 UART
- ERROR/Control Block

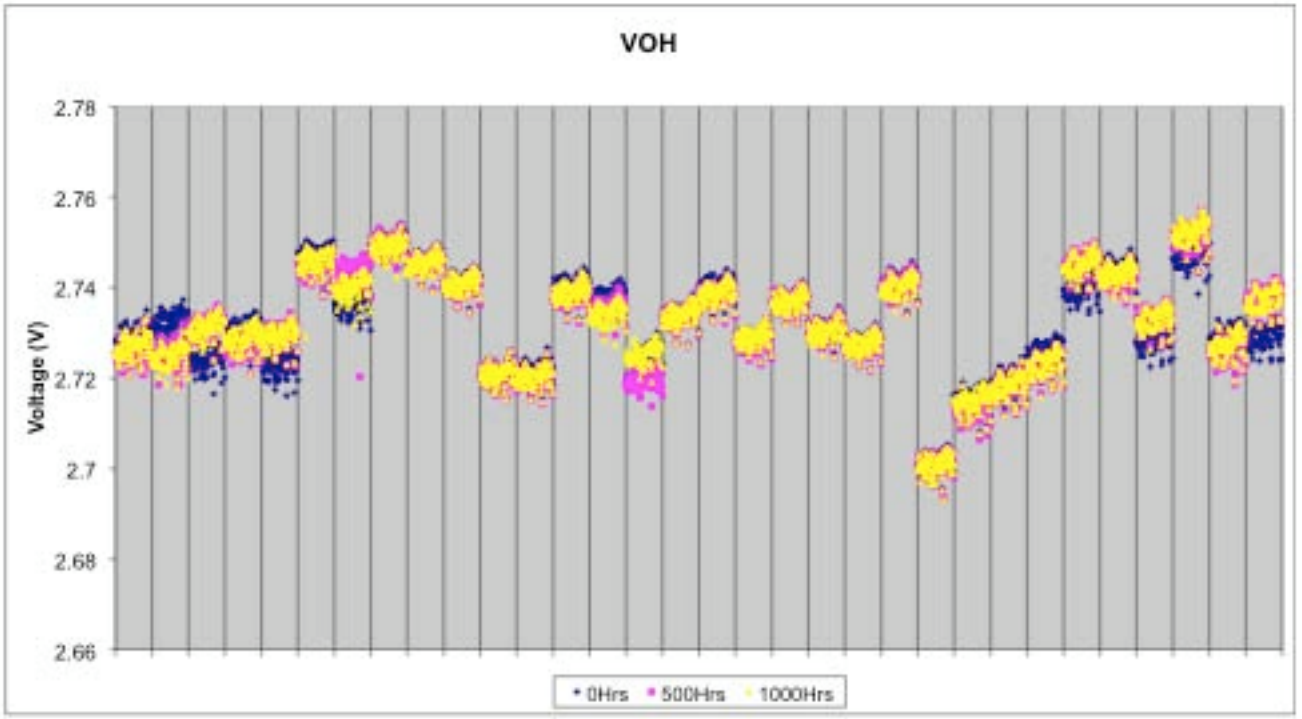
Combinational Cells:
1907 of 2816 (68%)
Sequential Cells
810 of 1408(58%)
Total Cells:
2717 of 4224 (65%)
Clock Buffers: 7
IO Cells: 28



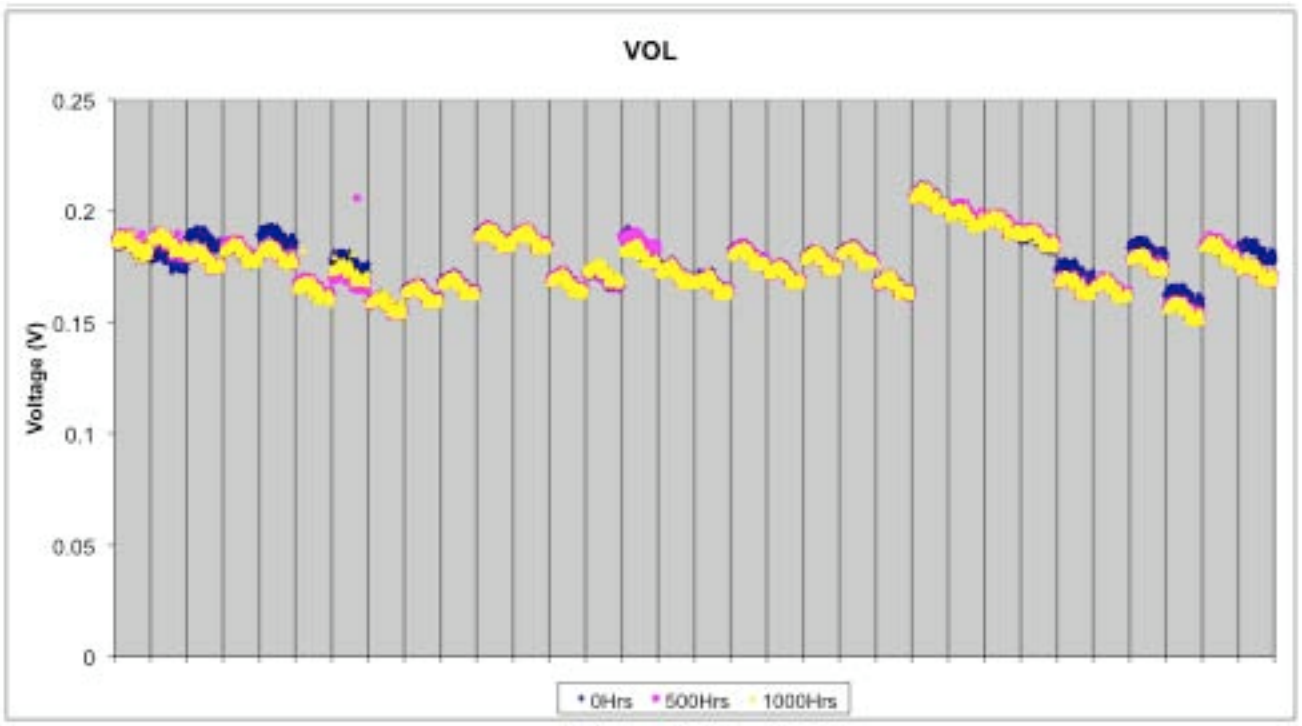
Status

- **As of September 2008**
  - Design review was held with Actel in Feb 08
  - Programming was completed by June 08
    - 2 - 250s and 5 - 2000s failed to program … replaced by Actel
  - Parts began testing at Actel contract facility mid-June
  - Pulled and tested at 500 and 1000 hour points
- No Failures
- No anomalous data

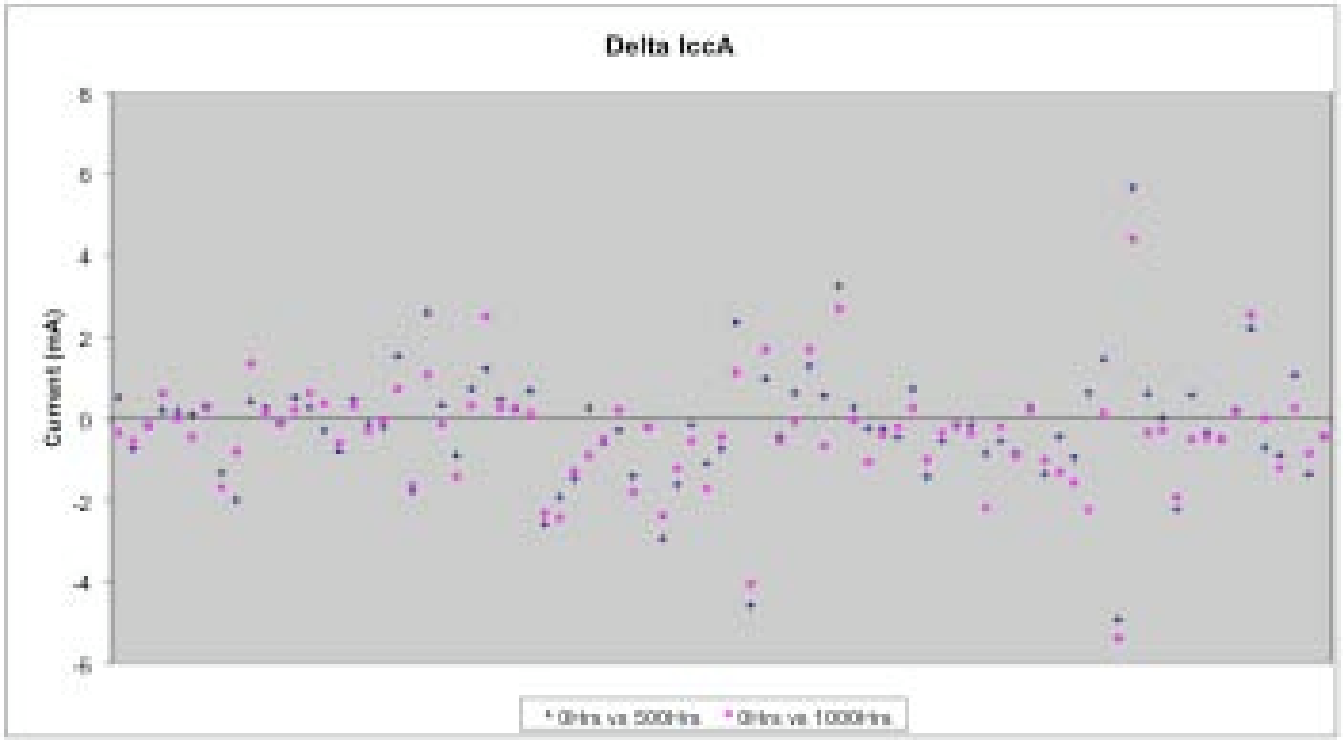
Test Data - VOH



Test Data - VOL

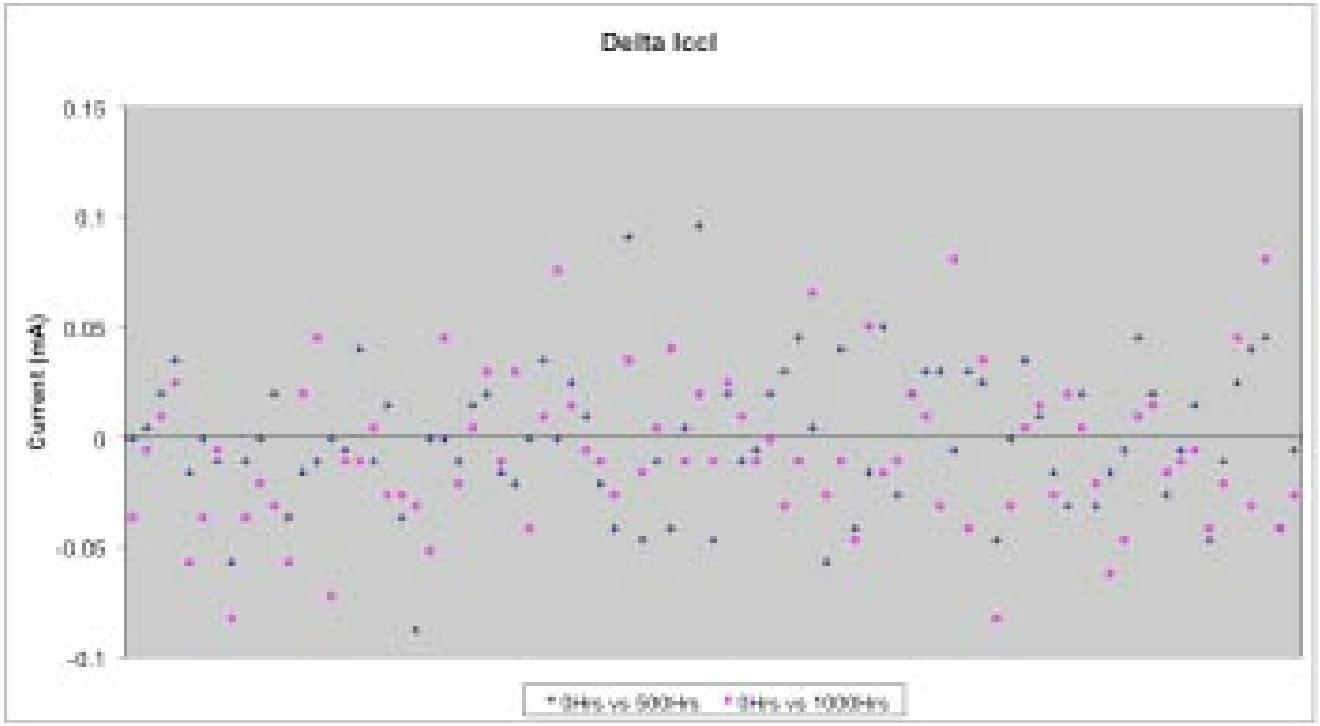


Test Data – Delta IccA



Change in Core Current

Test Data – Delta IccI



Change in I/O Current

NESC Assessment Team

Team Members

Mitchell Davis (LaRC) – Lead, NESC Power & Avionics Discipline Expert
Glenn Lindamood (GRC)
Douglas Sheldon (JPL)
Kosta Varnavas (MSFC)
Robert Lebair (GSFC)
Coy Kouba (JSC)
Tak-kwong Ng (LaRC)

Consultants

Michael Sampson (NEPP)
Lawrence Hatzstark (Aerospace Corp.)
Martin Fraeman (APL)
Jerry Soden (Sandia)
Daniel Yuchnovicz (LaRC)
Brian Smith (Stargazer Systems)
Greg Alkire (Stargazer Systems)

Contact:
Brian Smith
Bsmith@StargazerSystems.com
1783 Forest Drive, Suite 291
Annapolis, Maryland, 21401
301.358.2582